

Description

METHOD FOR FORMING INTERCONNECTS ON THIN WAFERS

BACKGROUND OF INVENTION

[0001] FIELD OF THE INVENTION

[0002] The present invention relates to the field of semiconductor processing; more specifically, it relates to a method of forming a solder interconnect structure on a thin wafer.

[0003] BACKGROUND OF THE INVENTION

[0004] Increasing density of semiconductor devices has allowed semiconductor chips to decrease in area. Along with the decrease in chip area, has come a need to make the semiconductor chips thinner. Current methods of thinning semiconductor wafers often lead to damage of the semiconductor chips.

SUMMARY OF INVENTION

[0005] A first aspect of the present invention is a method of forming a semiconductor interconnect comprising, in the order recited: (a) providing a semiconductor wafer; (b) forming bonding pads in a terminal wiring level on the frontside of the wafer; (c) reducing the thickness of the wafer; (d) forming solder bumps on the bonding pads; and (e) dicing the wafer into bumped semiconductor chips.

[0006] A second aspect of the present invention is a method of forming a semiconductor interconnect comprising, in the order recited: (a) providing a semiconductor wafer; (b) forming bonding pads in a terminal wiring level on the frontside of the wafer; (c) reducing the thickness of the wafer to produce a reduced thickness wafer; (d) providing an evaporation fixture comprising a bottom ring, a shim, an evaporation mask and a top ring; (e) placing the shim into the bottom ring; (f) placing the reduced thickness wafer on the shim; (g) placing on and aligning the mask to the reduced thickness wafer; (h) placing said top ring over said mask and temporarily fastening said top ring to said bottom ring; (i) evaporating solder bumps on the bonding pads through the mask; (j) removing the reduced thickness wafer from the fixture; and (k) dicing the reduced thickness wafer into bumped semiconductor chips.

[0007] A third aspect of the present invention is A fixture for holding wafer and an evaporative mask comprising: a bottom ring having a inner periphery and an outer periphery, the bottom ring having a raised inner lip formed along the inner periphery and a raised outer lip formed along the outer periphery, the height of the inner lip above a surface of the bottom ring being greater than a height of the outer lip above the surface of the bottom ring; a shim having a inner and an outer periphery, the outer periphery of the shim fitting inside and in proximity to the outer lip of the bottom ring, a bottom surface of the shim proximate to the inner periphery of the shim contacting an upper surface of the inner lip of the bottom ring; a top ring having an inner periphery and an outer periphery, the top ring having a lower raised lip formed along the inner periphery of the bottom ring and extending below a bottom surface of the top ring; and the bottom ring and the top ring adapted to press a bottom surface of the wafer against an upper surface of the shim

and to press a top surface of the wafer against a bottom surface of the mask
and to press a top surface of the mask proximate to the periphery of the
mask against a lower surface of the lower raised lip of the top ring.

BRIEF DESCRIPTION OF DRAWINGS

[0008] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0009] FIGs. 1A through 1F are partial cross-sectional views of the fabrication of a semiconductor wafer according to the present invention;

[0010] FIG. 2 is a cross-sectional view through an interconnect structure formed by the present invention;

[0011] FIG. 3A is a top view of a base portion of a wafer to mask alignment fixture for forming interconnects according to the present invention;

[0012] FIG. 3B is a cross-section view through line 3B-3B of FIG. 3A;

[0013] FIG. 4 is a top view of an evaporative mask portion of the wafer to mask alignment fixture for forming interconnects according to the present invention;

[0014] FIG. 5A is a top view of a top portion of the wafer to mask alignment fixture for forming interconnects according to the present invention;

[0015] FIG. 5B is a cross-section view through line 5B-5B of FIG. 5A;

[0016] FIG. 6A is a top view of a shim portion of a wafer to mask alignment fixture for forming interconnects according to the present invention;

[0017] FIG. 6B is a cross-section view through line 6B-6B of FIG. 6A;

[0018] FIG. 7 is a partial cross-section view through the assembled wafer to mask alignment fixture for forming interconnects according to the present invention; and

[0019] FIG. 8 is a partial cross-section view through the assembled wafer to mask alignment fixture for forming interconnects illustrating dimensional relationships between the component parts of the wafer to mask alignment fixture according to the present invention.

DETAILED DESCRIPTION

[0020] For the purposes of the present invention, the terms substrate and wafer may be used interchangeably.

[0021] FIGs. 1A through 1F are partial cross-sectional views of the fabrication of a semiconductor wafer according to the present invention. In FIG. 1A, a substrate *100* such as a semiconductor bulk silicon substrate or a semiconductor silicon-on-insulator (SOI) substrate has a thickness *T1*. Formed in/on substrate *100* is a multiplicity of active Field effect transistors (FETs) *105*. FETs *105* include gate electrodes *115* formed over gate dielectric formed *116* and between spacers *117* on a top surface *110* of substrate *100* and source/drains *118* formed in the substrate. FETs *105* are exemplary of devices and structures normally found in semiconductor circuits of semiconductor chips and many other structures and devices such as

capacitors, resistors, inductors, bipolar transistors and diffused and dielectric isolation. FETs *105* are wired into circuits in a first wiring level *120A*, a second wiring level *120B*, a third wiring level *120C* and a terminal wiring level *120D*. First wiring level contains contacts *125* interconnecting FETs *105* to conductors *125B* in second wiring layer *120B*. Conductors *125B* are in turn connected to conductors *125C* in third wiring level *120C*. Conductors *125C* are in turn connected to terminal conductors *125D* in terminal wiring level *120D*. Terminal conductors *125D* include a multiplicity of bonding pads *130*. Bonding pads *130* are exposed on surface *135* of terminal wiring layer *120D*. First wiring level *120A*, second wiring level *120B*, third wiring level *120C* and terminal wiring level *120D* are exemplary of wiring levels found in semiconductor chips and more or less wiring levels fabricated by any number of methods well known in the art such as subetch, liftoff, damascene and dual damascene may be used. Substrate *100* has a backside surface *140*.

[0022] In FIG. 1B, wafer *100A* is reduced from thickness T_1 (see FIG. 1A) to a new thickness T_2 (where $T_1 > T_2$) by any number of wafer thinning techniques well known in the art. In a first example, backside surface *140* (see FIG. 1A) is ground down to a new backside surface *145* by grinding the backside surface with a rotating diamond grindstone. In a second example, backside surface *140* (see FIG. 1A) is etched down to new backside surface *145* by etching the backside surface with a mixture of hydrofluoric and nitric acids while rotating the wafer. In a third example, backside surface *140* (see FIG. 1A) is lapped down to new backside surface *145* by introducing a slurry containing abrasive particles between the backside of the wafer and a rotating wheel. In a fourth example, backside surface *140* (see FIG. 1A) is

chemical-mechanical-polished (CMP) down to new backside surface 145 by introducing a slurry containing abrasive particles mixed with a silicon etchant solution between the backside of the wafer and a rotating wheel.

[0023] In one example of thinning, a 200 mm diameter wafer having an initial thickness T1 of about 650 to 780 microns is thinned to a new thickness T2 of about 150 to 450 microns. The present invention may be practiced using any diameter wafer including 100 mm, 125 mm and 300 mm wafer of any initial thickness T1, reducing the wafer to any final thickness T2 as required by the use of the finished chip.

[0024] In FIG. 1C an evaporative mask 150 having openings 155 is placed on top surface 135 (or very close to top surface 135) of terminal wiring level 120D. Openings 155 are aligned to bonding pads 130. Openings 155 have inner knife-edges 160. Evaporative mask 150 is typical of the type of mask used to fabricate controlled collapse chip connection (C4) interconnect structures. C4 interconnect structures are also known as solder bump interconnections. In one example, mask 150 is made from molybdenum.

[0025] In FIG. 1D, a pad limiting metallurgy (PLM) 165 is evaporated through opening 155 onto bonding pads 130. PLM 165 is discussed more fully *infra* in reference to FIG. 2. PLM is also known as ball limiting metallurgy (BLM).

[0026] In FIG. 1E, mask 150 is not moved and a solder bump 170 is evaporated through opening 155 onto PLM 165. Solder bump 170 has the shape of a truncated cone.

[0027] In FIG. 1F, mask 150 (see FIG. 1E) is removed and a reflow anneal is

performed in order to reshape solder bumps 170 into semi-spherical solder bumps (also known as solder balls or C4 balls) 170A. Solder bumps 170A are discussed more fully *infra in reference to FIG. 2*.

[0028] FIG. 2 is a cross-sectional view through an interconnect structure formed by the present invention. In FIG. 2, terminal wiring level 120D includes bonding pad 125D embedded in a dielectric layer 175. In one example, bonding pad 125D is aluminum, copper or alloys thereof. Formed on top of dielectric layer 175 is an optional capping layer 180. In one example, capping layer 180 is silicon nitride. Formed on top of capping layer 180 is an optional passivation layer 185. In one example, passivation layer 185 is silicon dioxide, silicon nitride, silicon oxynitride or combinations thereof. Formed on top of passivation layer 185 is an optional dielectric layer 190. In one example, dielectric layer 190 is polyimide. An optional via 195 is provided through capping layer 180, passivation layer 185 and dielectric layer 190 exposing bonding pad 125D in terminal wiring level 120D. Via 195 may be formed by any number of well known plasma etch techniques. PLM 165 is formed over dielectric layer 190, sidewalls of via 195 and exposed portions of terminal wiring level 120D. In one example, PLM 165 is titanium nitride, copper, gold, titanium-tungsten, chrome, chrome-copper or combinations thereof. A typical combination is gold over copper over chrome. Another typical combination is copper over chrome copper over titanium-tungsten. PLM 165 is in electrical contact with bonding pad 130. C4 ball 170A is formed on and in electrical contact with PLM 165. Examples of C4 ball 170A compositions include but are not limited to 95% lead and 5% tin, 97% lead and 3% tin, 100% lead, other lead alloys, 100% tin and tin alloys. In one example, the reflow anneal mentioned supra is performed at a temperature of between about 350oC

[0029] The evaporation process for forming PLMs 165 and solder bumps 170 (see FIG. 1E) is performed by placing the semiconductor substrate in wafer to mask alignment fixture that allows alignment of mask 150 to thinned substrate 100A (see FIG. 1E). The evaporation process includes loading multiple wafer to mask alignment fixtures (with wafers and masks and in the case of the present invention, shims) into spaces in a dome of a multi-source evaporator and each material of PLM and then the solder pad are evaporated onto contacts pads on the wafer through holes in a mask. Such a wafer to mask alignment fixture is illustrated in FIGs. 3A, 3B, 4, 5A, 5B, 6A and 6B and described infra.

[0030] FIG. 3A is a top view of a base portion of a wafer to mask alignment fixture for forming interconnects according to the present invention and FIG. 3B is a cross-section view through line 3B-3B of FIG. 3A. In FIGs. 3A and 3B, a bottom ring 200 includes an outer lip 205 and an inner lip 210 joined by an integral plate portion 215. Inner lip 210 defines the extent of an opening 220 centered in bottom ring 200. Plate portion 215 includes a multiplicity of openings 225 and a multiplicity of retaining post holes 227. Opening 220 provides access for a wafer handling fixture (not shown) and openings 225 are for thermal expansion and heat retention control. Bottom ring 200 has a diameter D1 and opening 220 has a diameter D2. The inside distance between opposite points on outer lip 205 is D3. Outer lip 205 has a height H1 measured from a top surface 230 of plate portion 215 and inner lip 210 has a height H2 measured from the top surface of the plate portion. The difference in height between outer lip 205 and inner lip 210 is H3 where $H3 = H2 - H1$ and

H2 is greater than H1. In one example, for an standard un-thinned 200 mm diameter wafer about 650 microns thick, H2 is about 0.080 inches and H1 is about 0.073 inches, making H3 about 0.007 inches. H1 and H2 will vary based on wafer diameters and standard un-thinned wafer thickness.

[0031] FIG. 4 is a top view of an evaporative mask portion of the wafer to mask alignment fixture for forming interconnects according to the present invention. In FIG. 4, mask 250 includes a multiplicity of openings 255 arranged in groups 260. Each group 260 corresponds to a chip on a wafer that will be placed under mask 250 as illustrated in FIG. 7 and described infra. Mask 250 has a diameter of D1, the same as the diameter of bottom ring 200 illustrated in FIG. 3A and described supra. Mask 250 includes a multiplicity of retaining post holes 262.

[0032] FIG. 5A is a top view of a top portion of the wafer to mask alignment fixture for forming interconnects according to the present invention and FIG. 5B is a cross-section view through line 5B-5B of FIG. 5A. In FIGs. 5A and 5B, top ring 270 has a lower lip 275 protruding from a bottom surface 280 of the top ring. Lower ring 275 protrudes a distance H4. In one example, for a standard 200 mm diameter wafer having a thickness of about 650 microns, H4 is about 0.002 inches. Top ring 270 includes an opening 280 centered within ring 270. Top ring 270 has a diameter of D1, the same as the diameter of bottom ring 200 illustrated in FIG. 3A and described supra. Top ring 270 includes a multiplicity of retaining posts 282.

[0033] FIG. 6A is a top view of a shim portion of a wafer to mask alignment fixture for forming interconnects according to the present invention and FIG. 6B is a

cross-section view through line 6B-6B of FIG. 6A. In FIGs. 6A and 6B a shim 290 has an opening 295 centered within the shim. Shim 290 has a diameter D3A where D3A is just slightly smaller than D3, the inside distance between opposite points on outer lip 205 (see FIG. 3A). D3 is greater than the diameter of the wafer being held in the fixture. Opening 295 has a diameter D2 the same as the diameter of opening 220 of bottom ring 200 illustrated in FIG. 3A and described supra. Shim 290 has a thickness T3. Shim 290 includes a multiplicity of retaining post notches 297 in a perimeter 298 of the shim.

[0034] FIG. 7 is a partial cross-section view through the assembled wafer to mask alignment fixture for forming interconnects according to the present invention. In FIG. 7, only half of the assembled fixture 300 (about centerline 305) is illustrated. To load/assemble fixture 300, shim 290 is placed in bottom ring 200 (contacting inner lip 210), thinned substrate 100A is placed on shim 290, mask 250 is placed on thinned substrate 100A and top ring 270 is placed on mask 250. Mask 250 is pressed between top ring 270 and outer lip 205 of bottom ring 200 and lower lip 275 of the top ring presses on mask 250. The only portion of bottom ring 200 contacted by shim 290 is inner lip 210. Clips (not shown) hold assembled fixture 300 together. Also, alignment pins and alignment holes in bottom and top rings 200 and 270 and alignment holes in mask 250 and shim 290 are present but not illustrated in FIG. 7. The combination of the difference in heights between outer and inner lips 205 and 210 of bottom ring 200 and the height of lower lip 275 of top ring 270 deflects (or bows) shim 290, substrate 100A and mask 250 into very shallow but semi-spherical shapes by pressing the peripheries of mask 250 and substrate 100A towards bottom ring 200. The degree of deflection of substrate

100A is D4 measured along the top surface of substrate 100A. The bow imparted to substrate 100A prevents or reduces such problems associated with evaporation through an knife edge opening in a mask such as sputter haze, PLM flaring and solder pad haloing.

[0035] Retaining post 282 passes through retaining post hole 262 in mask 250, retaining post notches 297 in shim 290 and retaining post hole 227 in bottom ring 200. A spring clip 310 engages retaining post 305 and temporarily fastens assembled fixture 300 together.

[0036] FIG. 8 is a partial cross-section view through the assembled wafer to mask alignment fixture for forming interconnects illustrating dimensional relationships between the component parts of the wafer to mask alignment fixture according to the present invention. The dimensions H1, H2 of outer and inner lips 205 and 210 of bottom ring 200 and the dimension H4 of lower lip 275 of top ring 270 (see FIG 5A) are experimentally determined for each combination of wafer diameter and standard un-thinned wafer thickness. Note it is possible that one wafer manufacturer may produce standard 200 mm diameter wafers that are 780 microns thick, while another manufacturer may produce standard 200 mm diameter wafers that are 640 microns thick. Either two sets of fixtures having different values of H1, H2 and H4 are required, or 640 micron thick wafers are treated as thin wafers compared to the 780 micron thick wafers and a single fixture is designed for 780 micron thick wafers. There are two methods of determining the thickness T3 for shim 290. The first method is to use the formula T3 (shim thickness) equals T1 (un-thinned or standard wafer thickness that fixture is designed for) minus T2 (thinned wafer thickness). For example, assume a fixture designed for a

200 mm diameter 640 micron thick having values of 0.073 for H1, 0.080 for H2 and 0.002 for H4. If the wafer has been thinned to 250 microns, then T3 will be 390 microns ($640-250=390$) even if the original thickness of the wafer was greater than 640 microns. If the fixture had been designed for a 780 micron thick wafer than shim 290, in the present example, would be 530 microns ($720-250=530$) thick.

[0037] The second method is to experimentally determine for a given thinned wafer thickness (T2) a shim thickness (T3) that yields the same wafer deflection (D4) (see FIG. 7) as the un-thinned standard wafer (of thickness T1) that the fixture was designed for. For example assume a fixture designed for a 200 mm diameter 640 micron thick having values of 0.073 for H1, 0.080 for H2 and 0.002 for H4. If the wafer has been thinned to 250 microns, then T3 will be selected from an experimentally determined table of shim thickness (T3) versus thinned wafer thickness (T2) versus wafer deflection (D4) to give the same wafer deflection (D4) with a shim in place as a 640 micron thick wafer even if the original thickness of the wafer was not equal to 640 microns.

[0038] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.